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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,461	07/29/2003	Tetsuya Matsuura	67160-014	4840

7590 09/29/2004

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EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,461	MATSUURA ET AL.	
	Examiner	Art Unit	
	Matthew E Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/29/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

Claim 3 is objected to because of the following informalities: the claim contains the limitations of "the respective spacers" in line 3, "the sequence" in line 4, "the opposite sides" in line 6, "the portions" lines 6-7, "the same" in line 8, and "said semiconductor devices" in line 10. There is insufficient antecedent basis for the limitations in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 recites the limitation "for each of said semiconductor devices" in line 10. There is insufficient antecedent basis for this limitation in the claim. The limitation in question is confusing because it seems that there are a plurality of first and second

semiconductors mounted on a plurality of first and second spacer substrates. Because the is insufficient antecedent basis for the term "each of said semiconductor devices" it is difficult to determine how the spacer substrate is split if there is only one first and second semiconductor mounted on one spacer substrate.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Akihiko (JP 11-112121 A).

Claims 1-3, as far as understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Takahashi et al. (US 6,025,648).

In re claim 1, Takahashi et al. shows (fig. 1) a semiconductor device comprising a first semiconductor comprising a substrate (1 middle), and a semiconductor chip (9) disposed on the major surface of said substrate and sealed with a resin (6 not labeled in the middle); a wiring board (1 bottom substrate), spacers (bump 7 on the bottom)

disposed between said wiring board and said substrate and connecting said first semiconductor to said wiring board electrically; and a second semiconductor (chip 2 bottom not labeled) electrically connected to said wiring board and disposed in the space formed by said wiring board said substrate, and said spacer.

In re claim 2, Takahashi et al. shows (fig. 1) that a plurality (chips 2 on each level) of said semiconductors are disposed on said wiring board.

In re claim 3, as far as understood, Takahashi et al. discloses (fig. 1 and col. 3, line 46 -lines 34) a method of manufacturing a semiconductor device comprising: mounting a first semiconductor (2) on the respective spacers (7) of a spacer substrate (1) , formed by with a plurality of spacers for a semiconductor device; mounting a second semiconductor (2 middle) on the opposite sides of the portions of the respective spacers whereon the first spacer has been connected and in the same direction of the first semiconductor, respectively.

Claims 1 and 2 are rejected under 35 U.S.C. 102(e) as being anticipated by Karnezos (US Pub. 2004/0113253 A1).

In re claim 1, Karnezos shows (fig. 2) a semiconductor device comprising a first semiconductor comprising a substrate (22), and a semiconductor chip (24) disposed on the major surface of said substrate and sealed with a resin (27); a wiring board (12), spacers (28) disposed between said wiring board and said substrate and connecting said first semiconductor to said wiring board electrically; and a second semiconductor

(14) electrically connected to said wiring board and disposed in the space formed by said wiring board said substrate, and said spacer.

In re claim 2, Karnezos shows (fig. 2) that a plurality (12 and 24) of said semiconductors are disposed on said wiring board.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Shin et al. (US 2004/0175916 A1), Ishii et al. (US 2002/0105091 A1), and Matsunami (US 2004/0175865 A1) also show semiconductor devices having stackable packages with spacers between them.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW
MEW
September 23, 2004

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
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